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Date of Filing	:	25 MAY 2000
Application Number	:	200002874-6
Applicant(s)	:	INSTITUTE OF MICROELECTRONICS
Title of Invention	:	INTEGRATED CIRCUIT INDUCTOR

CHIG KAM TACK
Assistant Registrar
for REGISTRAR OF PATENTS
SINGAPORE

PATENTS FORM 1

SECOND SCHEDULE
SINGAPORE
THE PATENTS ACT
(CHAPTER 221)
THE PATENTS RULES

Rule 19

200002874-6
25 MAY 2000

The Registrar of Patents
Registry of Patents

REQUEST FOR THE GRANT OF A PATENT

THE GRANT OF A PATENT IS REQUESTED BY THE UNDERSIGNED ON THE BASIS OF THE PRESENT APPLICATION.

I. Title of Invention		**INTEGRATED CIRCUIT INDUCTOR**			
II. Applicant(s) (See note 2)	*(a) Name*	**INSTITUTE OF MICROELECTRONICS**			
	Body Description/ Residency	A company limited by guarantee			
	Street Name & Number	11 Science Park Road, Singapore Science Park II			
	City				
	State				
	Country	SINGAPORE 117685			
	(b) Name				
	Body Description/ Residency				
	Street Name & Number				
	City				
	State				
	Country				
	(c) Name				
	Body Description/ Residency				
	Street Name & Number				
	City				
	State				
	Country				
III. Declaration of priority (see note 3)	*Country/Country Designated*		*File no.*		
	Filing Date				
	Country/Country Designated		*File no.*		
	Filing Date				
	Country/Country Designated		*File no.*		
	Filing Date				

SECOND SCHEDULE - continued

IV. Inventors (See note 4) (a) *The applicant(s) is/are the sole/joint inventor(s).*	☐ *Yes* ☒ *No*			
(b) *A statement on Patents Form 8 ~~is~~/will be furnished*	☒ *Yes* ☐ *No*			
V. Name of Agent (if any) (See note 5)	**ALLEN & GLEDHILL**			
VI. Address for Service (See note 6)	*Block/Hse No*	36	*Level No*	18
	Unit No/PO Box	01	*Postal Code*	068877
	Street Name	ROBINSON ROAD		
	Building Name	CITY HOUSE		
VII. Claiming an earlier filing date under section 20(3), 26(6) or 47(4). (See note 7)	*Application No*			
	Filing Date			
VIII. Invention has been displayed at an International Exhibition (See note 8)	☐ *Yes* ☒ *No*			
IX. Section 114 requirements *(See note 9)*	*The invention relates to and/or used a micro-organism deposited for the purposes of disclosure in accordance with section 114 with a depositary authority under the Budapest Treaty.* ☐ *Yes* ☒ *No*			

X. Check List (To be filled in by applicant or agent)			
A. The application contains the following number of sheet(s):-			
1. Request	**3**	*sheets*	
2. Description	**5**	*sheets*	
3. Claim(s).	**2**	*sheets*	
4. Drawing(s).	**5**	*sheets*	
5. Abstract.	**1**	*sheet*	
B. The application as filed is accompanied by:-			
1. Priority document			
2. Translation of priority document			
3. Statement of Inventorship & right to grant			
4. International Exhibition Certificate			

X. Signature(s) (See note 10)		
Applicant (a)		
Date	25 May 2000	
Applicant (b)		
Date		
Applicant (c)		
Date		

NOTES:

1. This form when completed, should be brought or sent to the Registry of Patents together with the prescribed fee and 3 copies of the description of the invention, and of any drawings.

2. Enter the name and address of each applicant in the spaces provided at paragraph II. Names of individuals should be indicated in full and the surname or family name should be underlined. The names of all partners in a firm must be given in full. The place of residence of each individual should also be furnished in the space provided. Bodies corporate should be designated by their corporate name and country of incorporation and, where appropriate, the state of incorporation within that country should be entered where provided. Where more than three applicants are to be named, the names and address of the fourth and any further applicants should be given on a separate sheet attached to this Form together with the signature of each of these further applicants.

3. The declaration of priority at paragraph III should state the date of the previous filing, the country in which it was made, and indicate the file number, if available. Where the application relied upon in an International Application or a regional patent application e.g. European patent application, one of the countries designated in that application [being one falling under the Patents (Convention Countries) Order] should be identified and the name of that country should be entered in the space provided.

4. Where the applicant or applicants is/are the sole inventor or the joint inventors, paragraph IV should be completed by marking the 'YES' Box in the declaration (a) and the 'NO' Box in the alternative statement (b). Where this is not the case, the 'NO' Box in declaration (a) should be marked and a statement will be required to be filed on Patents Form 8.

5. If the applicant has appointed an agent to act on his behalf, the agent's name should be indicated in the spaces available at paragraph V.

6. An address for service in Singapore to which all documents may be sent must be stated at paragraph VI. It is recommended that a telephone number be provided if an agent is not appointed.

7. When an application is made by virtue of section 20(3), 26(6) or 47(4), the appropriate section should be identified at paragraph VII and the number of the earlier application or any patent granted thereon identified.

8. Where the applicant wishes an earlier disclosure of the invention by him at an International Exhibition to be disregarded in accordance with section 14(4)(c), then the 'YES' box at paragraph VIII should be marked. Otherwise the 'NO' box should be marked.

9. Where in disclosing the invention the application refers to one or more micro-organisms deposited with a depository authority under the Budapest Treaty, then the 'YES' box at paragraph IX should be marked. Otherwise the 'NO' box should be marked.

10. Attention is drawn to rules 90 and 105 of the Patent Rules. Where there are more than three applicants, see also Note 2 above.

11. Applicants resident in Singapore are reminded that if the Registry of Patents considers that an application contains information the publication of which might be prejudicial to the defence of Singapore or the safety of the public, it may prohibit or restrict its publication or communication. Any person resident in Singapore and wishing to apply for patent protection in other countries must first obtain permission from the Singapore Registry of Patents unless they have already applied for a patent for the same invention in Singapore. In the latter case, no application should be made overseas until at least two months after the application has been filed in Singapore.

For Official Use

Application Filing Date: / /
Request received on : / /
Fee received on : / /
Amount :
*Cash/Cheque/Money Order No:

**Delete whichever is inapplicable*

2000028746
25 May 2000

INTEGRATED CIRCUIT INDUCTOR

The present invention relates to an integrated circuit inductor and a method of making the same.

An integrated circuit inductor is an inductive component built up on a substrate in a similar manner to other components, and generally includes a spiral conductive trace. This arrangement suffers from the disadvantage of high parasitic losses, in the form of resistive and capacitive losses to the semiconductor substrate on which the integrated circuit is built.

A solution to this problem is to selectively etch the silicon substrate beneath the conductive trace, as described in US patent specification No. 5,539.241. This solution is shown in the accompanying drawings, in which:

Figure 1 is a plan view of the prior integrated circuit inductor and

Figure 2 is a cross-sectional view on the line II-II in Figure 1 of the prior inductor.

The inductor 1 comprises a spiral aluminium track 2. It is laid down on a insulating oxide layer 3, which itself covers the semiconductor substrate 4. From its inner end 5, an underpass track 6 at a lower level in deposited layers making up the inductor passes from the inner end 5 to a connection 7. The other, outer end 8 is directly connected to another connection 9 at the same level. The spiral track 2 has a substantial extent. If spaced from the semiconductor substrate by the thickness of the insulating layer alone, which has a comparatively high dielectric value, the inductive track has an appreciable capacitive connection to the substrate and hence at high frequencies, the component is liable to lose its inductive effect and act as a capacitor.

In accordance with the improvement of the said US patent, the oxide layer

has apertures 10 formed in it, with a track supporting portion 11 connected to the surround layer by bridges 12. Via the apertures, the substrate is etched away, leaving an air gap 14 beneath the oxide portion 11. Thus the inductive track 2 is spaced from semiconductor, reducing its capacitive connection thereto, air having a low dielectric constant. Whilst this is a distinct improvement, the formation of the air gap 14 requires the use of aggressive chemicals and is a slow process. Further, the air gap can be formed only as a post fabrication step, because the liquid etchant required is not used in the CMOS fabrication.

The object of the invention is to provide an improved integrated circuit inductor and method of making the same.

According to the invention there is provided an integrated circuit inductor, the integrated circuit having a silicon substrate and an oxide layer on the silicon substrate, the inductor comprising:

an inductive loop deposited on the oxide layer;

apertures in the oxide layer beneath the inductive loop;

bridges adjacent the apertures and provided by portions of the oxide between an inner region and an outer region of the oxide layer, respectively within and without the inductive loop, the loop being supported on the bridges;

a trench formed in the silicon substrate beneath the bridges, to provide an air gap between the inductive loop and the silicon substrate.

Preferably, the apertures and the bridges extend generally radially of the inner region; and the trench extends circumferentially of the inner region.

Normally the inductive loop will have a plurality of spirally arranged turns; and the oxide layer includes an underpass connection in one of the bridges from a peripheral connection for one end of the inductor to its inner end.

According to another aspect of the invention there is provided a method of making an integrated circuit inductor, the integrated circuit having a silicon substrate

and an oxide layer on the silicon substrate, as claimed in claim 1, the method consisting in the steps of:

depositing the inductive loop on the oxide layer;

opening the apertures in the oxide beneath the inductive loop and providing the bridges to support the loop;

forming the trench in the silicon substrate beneath the bridges.

Preferably, the trench is formed by etching of the silicon substrate; and the etching is continued until the trench is continuous beneath the extent of the inductive loop.

To help understanding of the invention, a specific embodiment thereof will now be described with reference to the accompanying drawings, in which:

Figure 3 is a plan view of an integrated circuit inductor according to the invention;

Figure 4 is a cross-sectional view on the line IV-IV in Figure 3 of the inductor of the invention,

Figures 5(i) to 5(vii) are cross-sectional views similar to Figure 4, but on a larger scale, of steps in the production of the inductor of Figure 3;

Figure 6 is a perspective scrap view of a corner portion of the inductor of Figure 3.

Referring to Figures 3 and 4, in common with the prior inductor, the inductor 101 of the invention has a spiral aluminium track 102. It is deposited on an oxide layer 103 over the silicon substrate 104. The latter is etched away in a trench 114 which extends around the beneath the track, to provide a low dielectric air gap 115. The oxide 103 has an inner region 1031 within the track 102, an outer region 1032 outside the track and a bridging region 1033 extending between the other regions,

the bridging region being comprised of intact bridges 1034 and gaps 1035 therebetween, which open to the trench and through which the etchant had access to the silicon substrate for its etching to form the trench.

Referring now to Figures 5(i.) to 5(vii.), a first oxide layer 1036 is first laid down on the silicon substrate 104, with a first metal layer 106 on top. As shown in Figure 5(ii.), the metal is etched back to leave only a short track 1061, which will form an "underpass" connection to the inner end of the spiral track of the inductor. Additional oxide 1037 is deposited over the top of the bottom layer to at least temporarily enclose it in insulating material. Then, via a temporary mask 140, Figure 5(iv.), vias 141 are etched to the underpass track 1061. With the mask removed again, further metal 1021 is deposited to fill the vias and provide metal for the spiral track 102. For the definition of this. another mask 142 is laid down, see Figure 5(vi.) and the metal between the individual turns of the track is removed. The mask is removed. At this stage, the metal of the track is fully defined in an analogous manner to that of the prior art.

Now as shown in Figure 5(vii.), a further mask 143 is laid down, to etch away gaps 1035 in the oxide, that is in both the first and second layers 1036,1037, down to the silicon substrate 104, The bridges 1034 from the central region 1031 to the circumferential regions 1032 are left intact, with the conductive track 102 spanning from one bridge to the next. Finally, the silicon substrate beneath the gaps 1035 is etched away. The etching is continued until the voids formed beneath the track coalesce to form the trench 114.

Figure 6 shows a scrap view of the trench under a corner portion of the inductor.

Since the etching of the substrate is from directly above where the trench is to being formed, as opposed to from outside the inductor as in the prior art referred to above, no extra area is consumed. Further, the etching is fully CMOS compatible in the use of CMOS RIE tools and gases such as SF_6, He, O_2, etc.

The material details of the above steps are the same as those employed in CMOS technology, and as such are familiar to the man skilled in the art and will not be described in more detail. Certain of the described steps will be useful in the formation of other components elsewhere on the substrate; and indeed other steps may be incorporated in the process for forming components elsewhere without interfering with the formation of the inductor.

Utilising the invention, we have achieved an inductor with a low parasitic capacitance and a Q value of 15 at 1.9GHz.

CLAIMS

1. An integrated circuit inductor, the integrated circuit having a silicon substrate and an oxide layer on the silicon substrate, the inductor comprising:

an inductive loop deposited on the oxide layer;

apertures in the oxide layer beneath the inductive loop;

bridges adjacent the apertures and provided by portions of the oxide between an inner region and an outer region of the oxide layer, respectively within and without the inductive loop, the loop being supported on the bridges;

a trench formed in the silicon substrate beneath the bridges, to provide an air gap between the inductive loop and the silicon substrate.

2. An integrated circuit inductor as claimed in claim 1, wherein the apertures and the bridges extend generally radially of the inner region.

3. An integrated circuit inductor as claimed in claim 1 or claim 2, wherein the trench extends circumferentially of the inner region.

4. An integrated circuit inductor as claimed in claim 1, claim 2 or claim 3, wherein the inductive loop has a plurality of spirally arranged turns.

5. An integrated circuit inductor as claimed in any preceding claim, wherein the oxide layer includes an underpass connection in one of the bridges from a peripheral connection for one end of the inductor to its inner end.

6. A method of making an integrated circuit inductor, the integrated circuit having a silicon substrate and an oxide layer on the silicon substrate, as claimed in claim 1, the method consisting in the steps of:

depositing the inductive loop on the oxide layer;

opening the apertures in the oxide beneath the inductive loop and providing the bridges to support the loop;

forming the trench in the silicon substrate beneath the bridges.

7. A method as claimed in claim 6, wherein the trench is formed by etching of the silicon substrate.

8. A method as claimed in claim 6 or claim 7, wherein the etching is continued until the trench is continuous beneath the extent of the inductive loop.

ABSTRACT

INTEGRATED CIRCUIT INDUCTOR

An inductor 101 having a spiral aluminium track 102 deposited on an oxide layer 103 over the silicon substrate 104. The latter is etched away in a trench 114 which extends around the beneath the track, to provide a low dielectric air gap 115. The oxide 103 has an inner region 1031 within the track 102, an outer region 1032 outside the track and a bridging region 1033 extending between the other regions, the bridging region being comprised of intact bridges 1034 and gaps 1035 therebetween, which open to the trench and through which the etchant had access to the silicon substrate for its etching to form the trench.

(Figure 6)

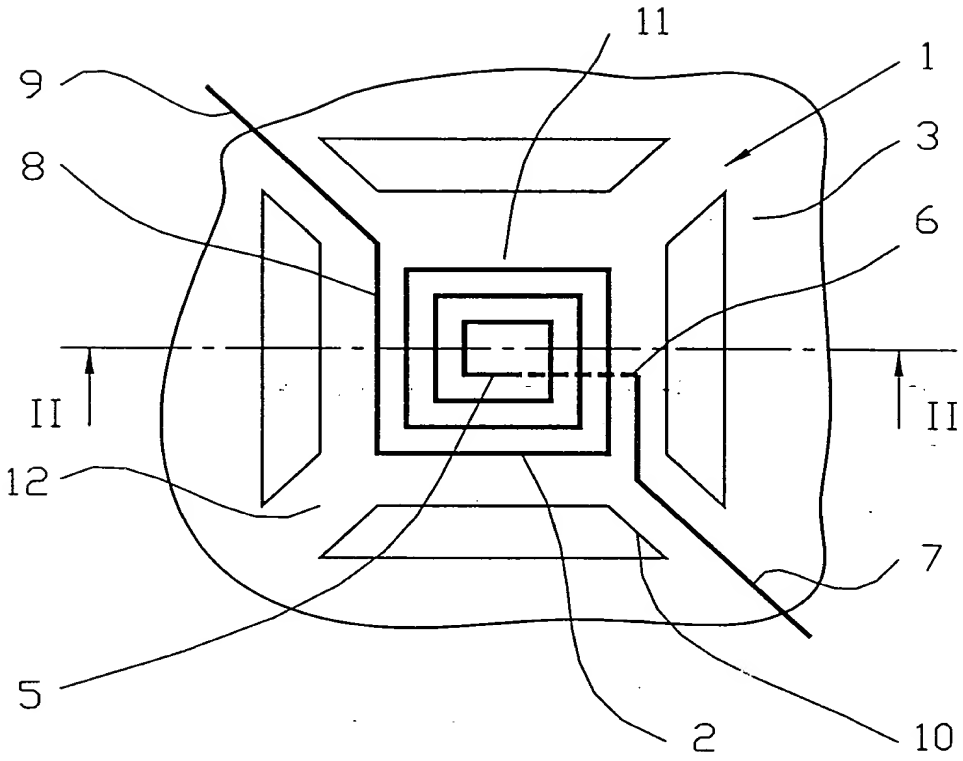

FIGURE 1

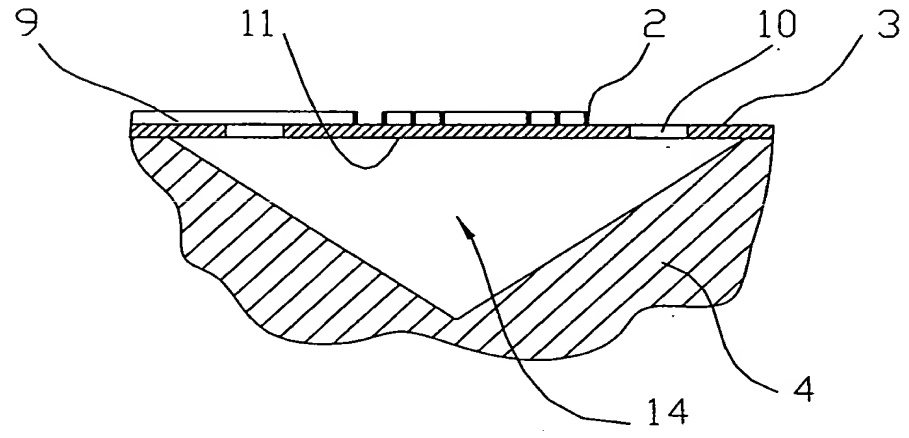

FIGURE 2

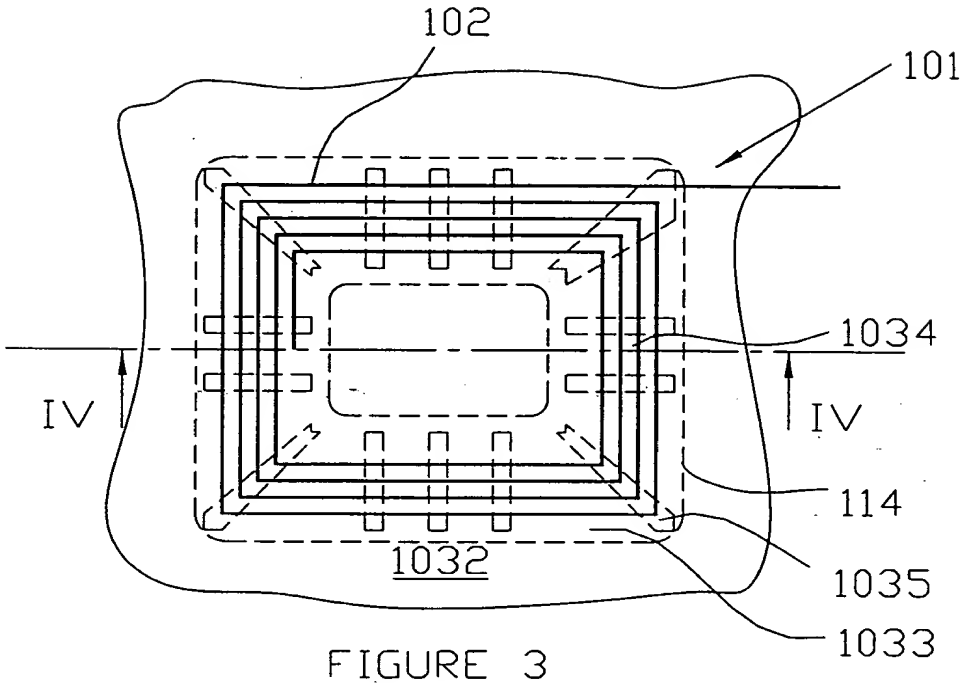

FIGURE 3

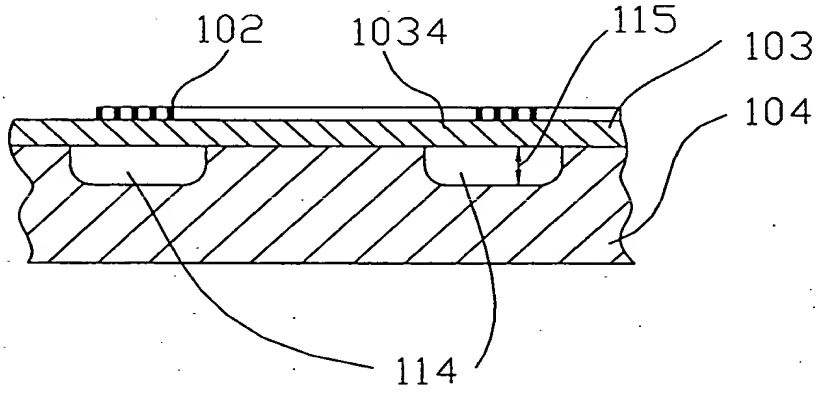

FIGURE 4

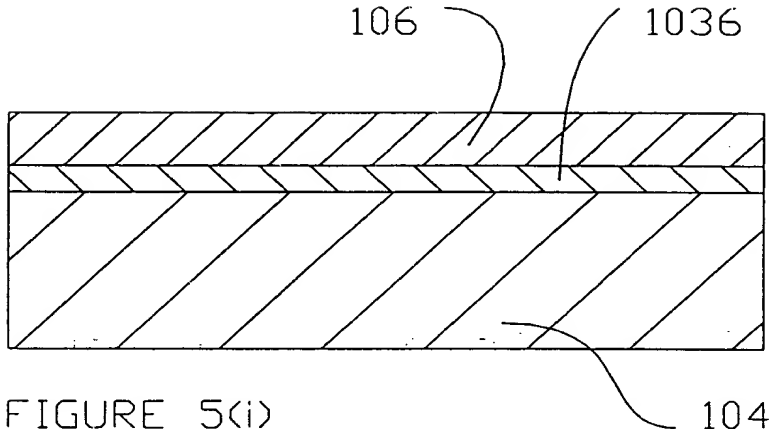

FIGURE 5(i)

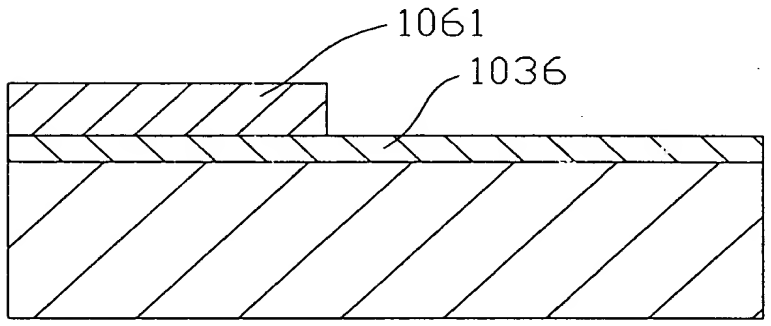

FIGURE 5(ii)

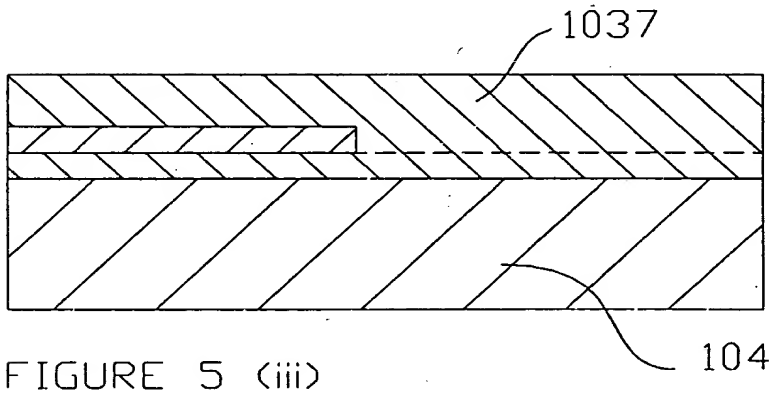

FIGURE 5 (iii)

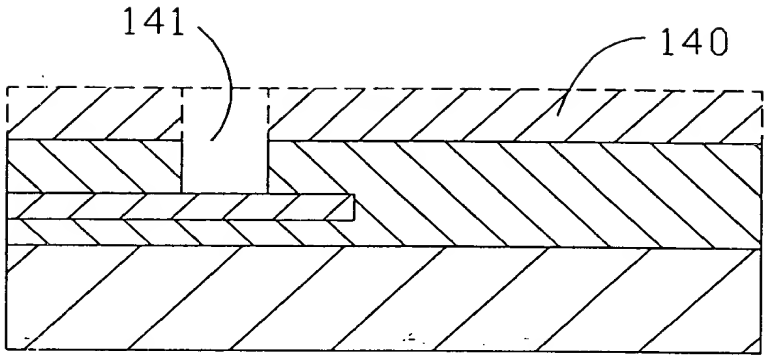

FIGURE 5(iv)

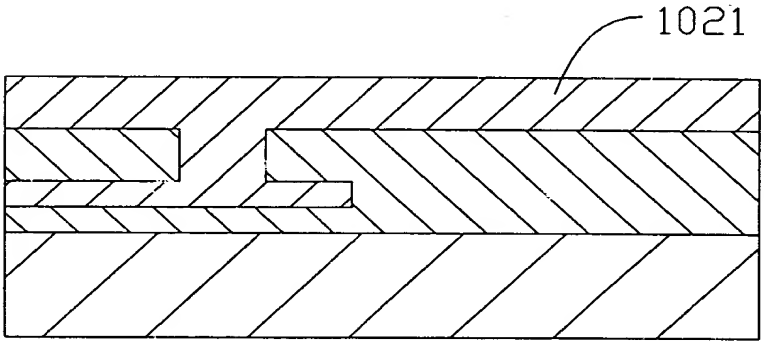

FIGURE 5(v)

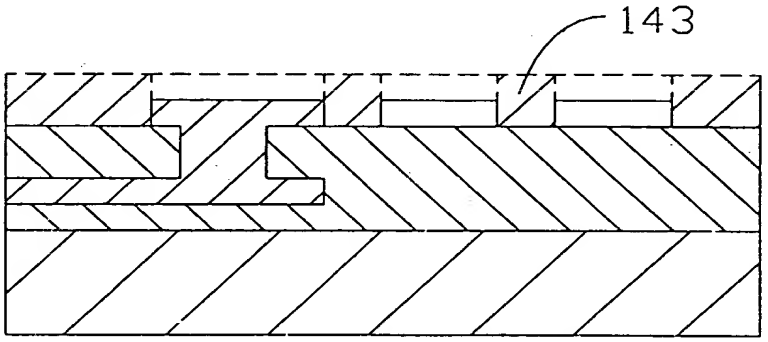

FIGURE 5 (vi)

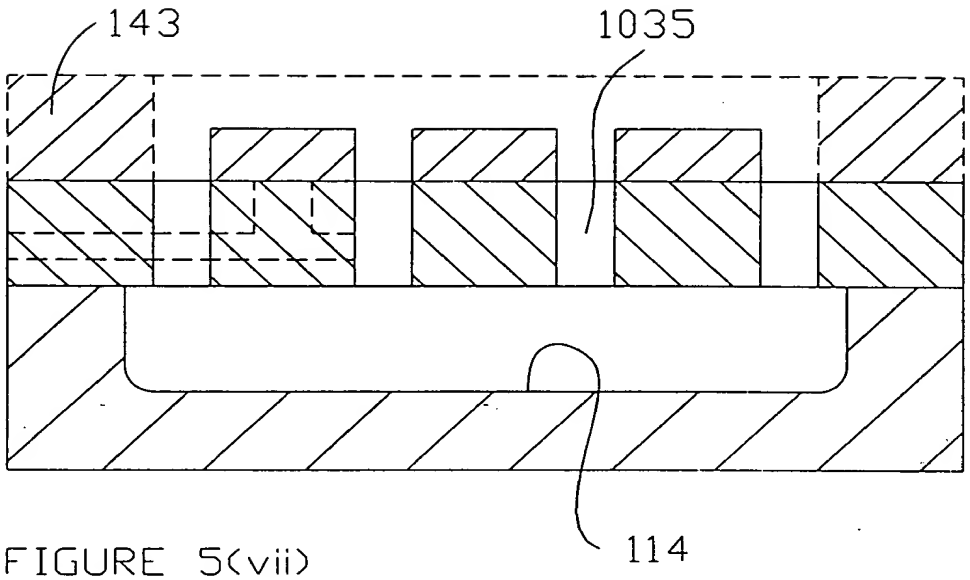

FIGURE 5(vii)

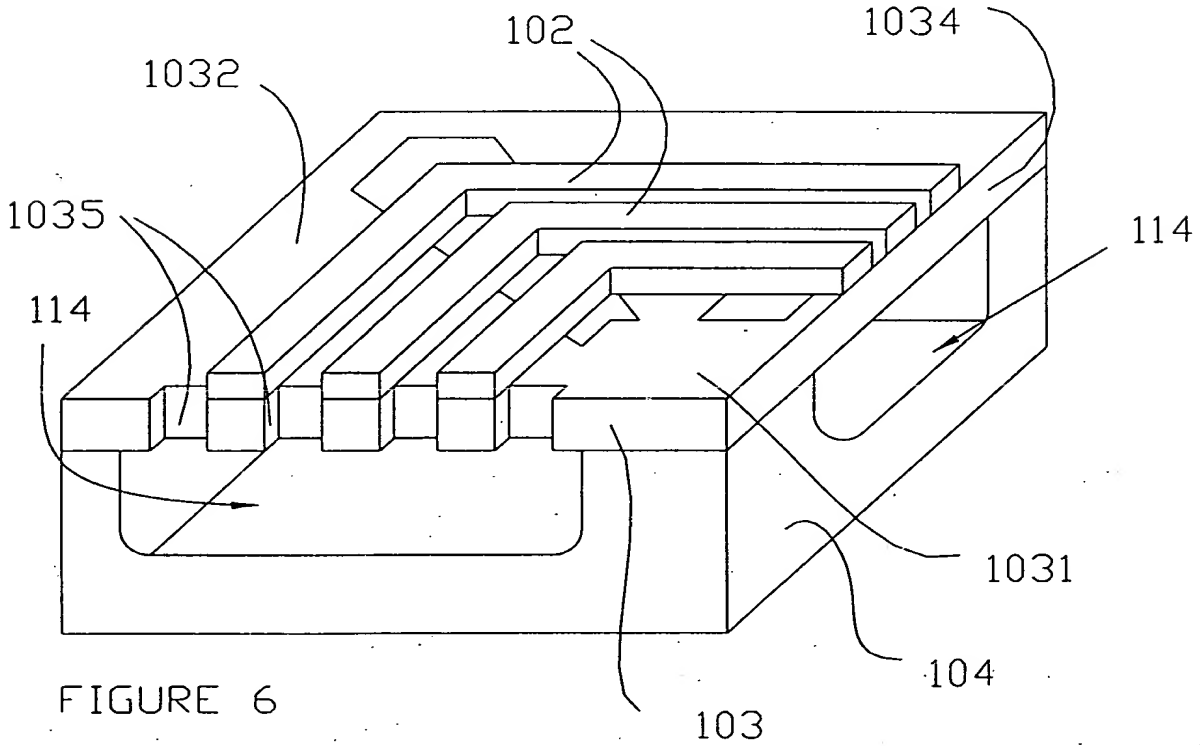

FIGURE 6